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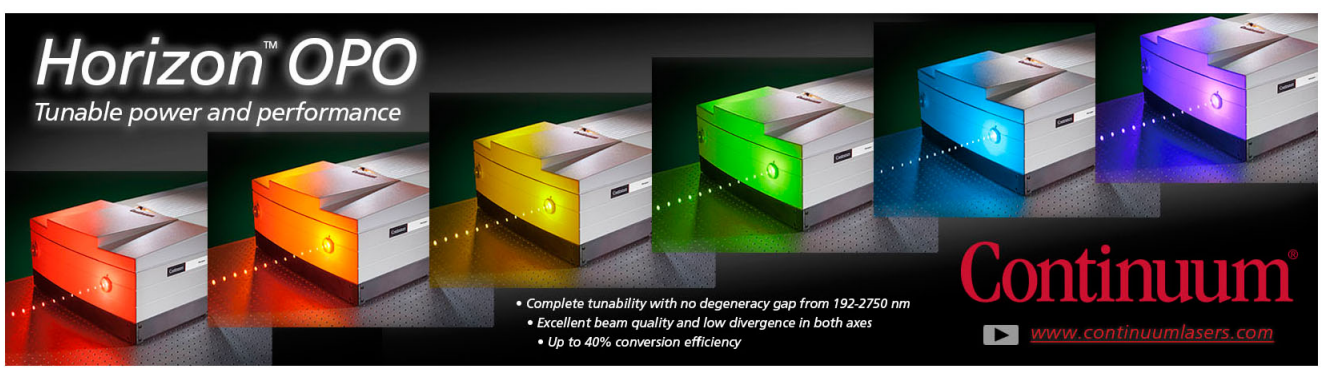

In-situ tuning threshold voltage of field-effect transistors based on blends of poly(3-hexylthiophene) with an insulator electret

Guanghao Lu,[1,2,3,a)] Norbert Koch,[1] and Dieter Neher[2]
[1]*Institut für Physik, Humboldt-Universität zu Berlin, Newtonstraße 15, 12489 Berlin, Germany*
[2]*Institut für Physik und Astronomie, Universität Potsdam, Karl-Liebknecht-Straße 24-25, 14476 Potsdam, Germany*
[3]*Frontier Institute of Science and Technology and State Key Laboratory of Electrical Insulation and Power Equipment, Xi'an Jiaotong University, Yanxiang Road 99, 710054 Xi'an, People's Republic of China*

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Blending the conjugated polymer poly(3-hexylthiophene) (P3HT) with the insulating electret polystyrene (PS), we show that the threshold voltage V_t of organic field-effect transistors (OFETs) can be easily and reversely tuned by applying a gate bias stress at 130 °C. It is proposed that this phenomenon is caused by thermally activated charge injection from P3HT into PS matrix, and that this charge is immobilized within the PS matrix after cooling down to room temperature. Therefore, room-temperature hysteresis-free FETs with desired V_t can be easily achieved. The approach is applied to reversely tune the OFET mode of operation from accumulation to depletion, and to build inverters. © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4928554]

In the last decades, the performance of conjugated polymer field-effect transistors (FETs) has been improved drastically, especially in terms of charge carrier mobility and on/off ratio. From the application point of view, low-voltage and narrow-spread threshold voltage V_t[1] are also highly desired features. Therefore, *in-situ* tuning of V_t of individual FETs within an entire chip after integrated circuit (IC) fabrication enables improved device reliability and performance. In addition, controlled shifting of V_t plays a key role in FET-based nonvolatile memory elements.[2] Moreover, FETs driven in the accumulation mode need to have a different V_t from those working in the depletion mode,[3] and ICs combining FETs working in both accumulation and depletion mode can replace p/n FET-based ICs in numerous applications.[4] Compared to neat macromolecular semiconductor, blends of conjugated polymers with an insulating matrix polymer have been used for organic FETs (OFETs) with low-cost fabrication procedures, high optical transparency, and outstanding flexibility.[5,6] Although the mobility of these blends has been improved towards 1 $cm^2\ V^{-1}\ s^{-1}$ or higher, *in-situ* tuning of the V_t is required for practical application of semiconductor/insulating-polymer blend FET.

Up to now, only a few methods have been proven to be able to reversibly tune V_t of organic FETs. Among these, the introduction of a polymer-electret layer as an analog of the floating-gate is an often-used concept.[7–9] In the commonly used layered-structure gate|dielectric|polymer-electret|semiconductor, where the polymer-electret layer is used to store charges, charges are originally injected from source/drain electrodes. Considering that the valence band (in the case of hole injection) onset E_V of the semiconductor is normally higher than that of the polymer-electret, the injection of charge from the semiconductor layer into the polymer-electret needs to overcome this barrier. In other words, the gate bias actually leads to an high electrical field across the polymer-electret layer, which pulls charge from the semiconductor towards the polymer-electret/dielectric interface, and stores these in the layer formed by the polymer electret. The net charges in the electret thus act as an analog of an extra "gate," which can shift V_t of the corresponding OFET. However, when polymer-electret layers[7,8,10,11] were used to store charge, in order to substantially change V_t at room temperature and at the same time to avoid an influence of the reading voltage on V_t, the required programming voltage was usually much higher than the reading voltage. On the other hand, unintentionally doping of organic semiconductor by ambient species (oxygen/water) also changes the threshold voltage; therefore, many of these devices are intrinsically unstable when exposed to air. We recently showed that this instability can be largely avoided by blending poly(3-hexylthiophene) (P3HT) with an insulating polymer (like polystyrene (PS)). In this case, the doping actually improves mobility and renders the device stable versus further air-exposure.[6]

Here, we use the insulating-matrix in such moderately doped P3HT:PS (5 wt. % P3HT in PS) blends as an electret, which allows one to store a sufficient amount of charge at elevated temperature to strongly impact the FET behavior. As these charges are immobilized within the PS matrix at room temperature, the so-formed transistors exhibit hysteresis-free current voltage characteristics at room temperature, while their V_t can be tuned over a wide range depending on the amount of trapped charge in the PS matrix. Taking advantage of this observation, we applied P3HT/PS blends to circuitry prototypes.

In this work, P3HT/PS (P3HT 5 wt. %) (P3HT, 98% head-to-tail regioregularity, $M_n = 32$ kDa, Polydispersity index (PDI) = 2.4, Sepiolid P200; PS, $M_w = 95$ kDa, $PDI = 1.1$, Fluka AG) blends films (thickness of 20–30 nm) were prepared via spincoating from *o*-dichlorobenzene solution onto 300 nm SiO_2 with n-doped silicon as gate. Such films show good topographical homogeneity.[6] After evaporation of Au as source/drain electrodes, the devices were placed in the glovebox

a)Author to whom correspondence should be addressed. Electronic mail: guanghao.lu@mail.xjtu.edu.cn.

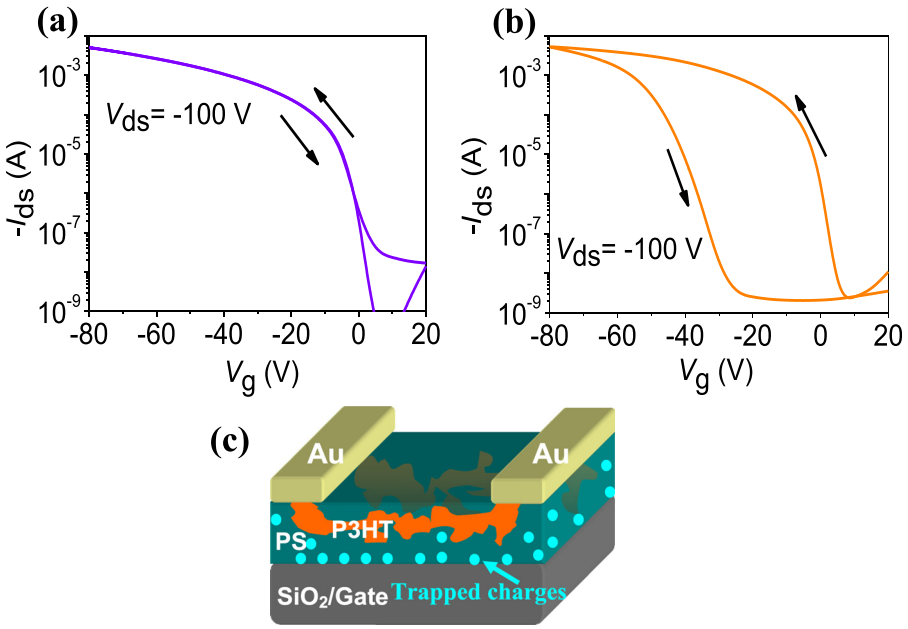

FIG. 1. (a) and (b) Transfer characteristics of P3HT/PS (5% P3HT) FET (scanning speed of 50 V/s) at room temperature (20 °C) (a) and at 130 °C (b), respectively. (c) Scheme of trapping charge by insulating-matrix electret.

overnight and were measured by an Agilent 4155C semiconductor parameter analyzer. These transistors comprise a bulk-distributed interface between a loosely connected network of nanocrystallites of the conjugated polymer and the insulating polymer.[6] Despite the presence of doped polymer domains, these polymers had a well-defined threshold voltage and a low off current, which we assign to the depletion of crystallites of the charge-transporting polymer nearest to the gate electrode.

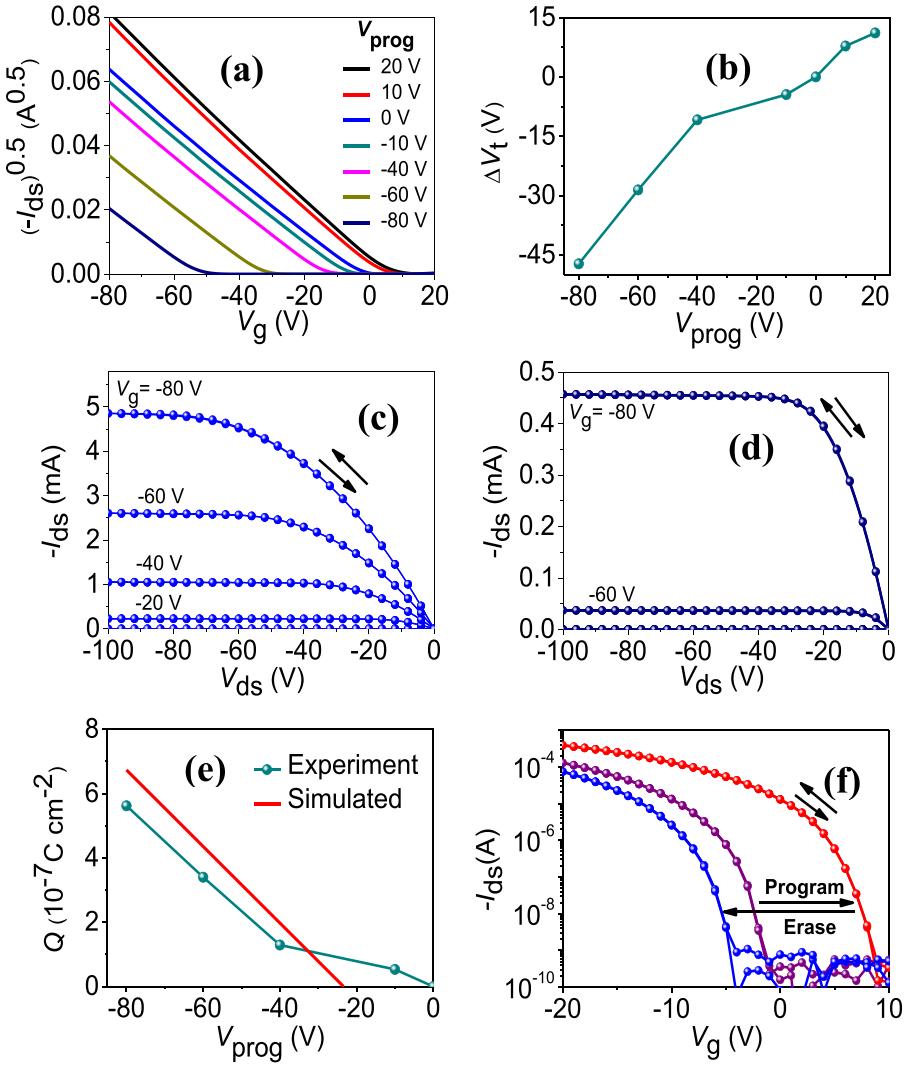

FIG. 2. Tuning the threshold voltage of P3HT/PS FET using different gate bias stresses (V_{prog}) at 130 °C. (a) Dependence of $(-I_{ds})^{0.5}$ on V_g for different V_{prog}. (b) The change of threshold voltage ΔV_t on V_{prog}. (c) and (d) Output characteristics after stress at $V_{prog} = 0$ V (c) and $V_{prog} = -80$ V (d) at 130 °C, respectively. (e) Charge density (Q) trapped in PS. The experimental data are obtained from Eq. (2). The slope of the simulated line is $\varepsilon_{SiO2}/d_{SiO2}$, and the critical gate bias for charge accumulation in PS electret is from Eq. (3). (f) Reversible change of the FET between enhancement and depletion mode. Enhancement to depletion mode: 130 °C for 1 min at $V_{prog} = 10$ V; and then from depletion to enhancement mode: 130 °C for 2 min at $V_{prog} = -30$ V. All curves were measured at room temperature.

Room temperature transfer curves of FETs are almost hysteresis free for source-drain current $I_{ds} > 10^{-7}$ A, while they show pronounced hysteresis at 130 °C, which is higher than glass transition temperature (90–110 °C) of PS (Figures 1(a) and 1(b)). This hysteresis implies a window as large as 30 V, which is a reminiscence of transistors using layered insulating polymer electrets.[7,8,10] As an analog of the mechanism commonly adopted in these layered polymer electrets, a scheme is proposed in Figure 1(c), where holes are stored (trapped) within the PS matrix during applying a negative gate bias at 130 °C.

Following this idea, we subjected FETs for programming by applying different gate biases[1,12] with source-drain voltage $V_{ds} = 0$ V during the entire process (heating, 130 °C/min; 130 °C for 1 min; cooling, 130 °C/min). Here, the programming voltage V_{prog} is defined as the gate bias V_g during the programming. The transfer characteristics measured at room temperature by following programming at V_{prog} ranging between 20 V and −80 V are shown in Figure 2(a). Negative V_{prog} substantially shifts the transfer curves towards negative direction, while positive V_{prog} induces positive-shifting. The square root of the source-drain current $(-I_{ds})^{0.5}$ is linear in V_g, meaning that the current I_{ds} obeys the well-known transistor equation $I_{ds} = (WC_i/2L)\mu_{sat}(V_g - V_t)^2$, where C_i (11.9 nF cm^{-2}) is the capacitance per unit area; L (100 μm) is the channel length; and W (148.5 mm) is the channel width. μ_{sat} is the saturation mobility, which is ca. 0.1–0.2 cm^2 V^{-1} s^{-1} for P3HT/PS (5% P3HT) blends in this work and fairly independent of gate bias. Noteworthy, the slope of $(-I_{ds})^{0.5}$ *vs.* V_g does not significantly change for different V_{prog}, meaning that the saturation mobility remains unaffected by gate bias stress. Extrapolating the linear range of $(-I_{ds})^{0.5}$ versus V_g yields the threshold voltage V_t for each programming voltage. We find that our procedure allows changing V_t by almost up to 60 V, from +5 V to −52 V. This observation further confirms the mechanism proposed in Fig. 1(c), where the stored charge in the PS matrix offsets the gate bias in the transfer characteristics. The output characteristics (Figures 2(c) and 2(d)) confirm that room temperature devices work without obvious hysteresis, meaning that the charge in the PS remains immobile at room temperature. As a consequence, the FET properties can be tuned by applying a suitable gate bias at elevated temperature, while these properties can be frozen into a stable state after cooling down to room temperature.

Considering the net charge density Q immobilized in the PS matrix, V_g should be replaced by V_g-$Q/C_{SiO2} = V_g$-$d_{SiO2}Q/\varepsilon_{SiO2}$ in the equation $I_{ds} = (WC_i/2L)\mu_{sat}(V_g - V_t)^2$, yielding

$$|I_{ds}|^{1/2} = \left(\frac{WC_{SiO_2}}{2L}\mu\right)^{1/2}\left(V_g - \frac{d_{SiO_2}Q}{\varepsilon_{SiO_2}} - V_t\right). \quad (1)$$

Obviously, $|I_{ds}|^{1/2}$ still scales linearly with V_g, while the intercept with the V_g axis strongly depends on charge density Q stored in PS matrix, which can be estimated from the change of threshold voltage ΔV_t

$$Q = \frac{\varepsilon_{SiO_2}}{d_{SiO_2}}\Delta V_t. \quad (2)$$

The dependence of Q on V_{prog} at 130 °C is shown in Figure 2(e). Obviously, at low $|V_{prog}|$, the charge accumulated in the PS matrix increases slightly with $-V_{prog}$, Notably, the amount of trapped charge increases more strongly with increasing $|V_{prog}|$ at higher programming voltage, implying efficient trapping in the PS electret.

In our previous publication,[6] we found that most P3HT are enriched at the top part of the blend; we simplify the P3HT/PS (5% P3HT) film as a two sub-layer system composed of a pure P3HT layer and a pure PS layer. The PS layer features a much deeper valence band than that of P3HT. When the gate voltage raises the PS valence band at

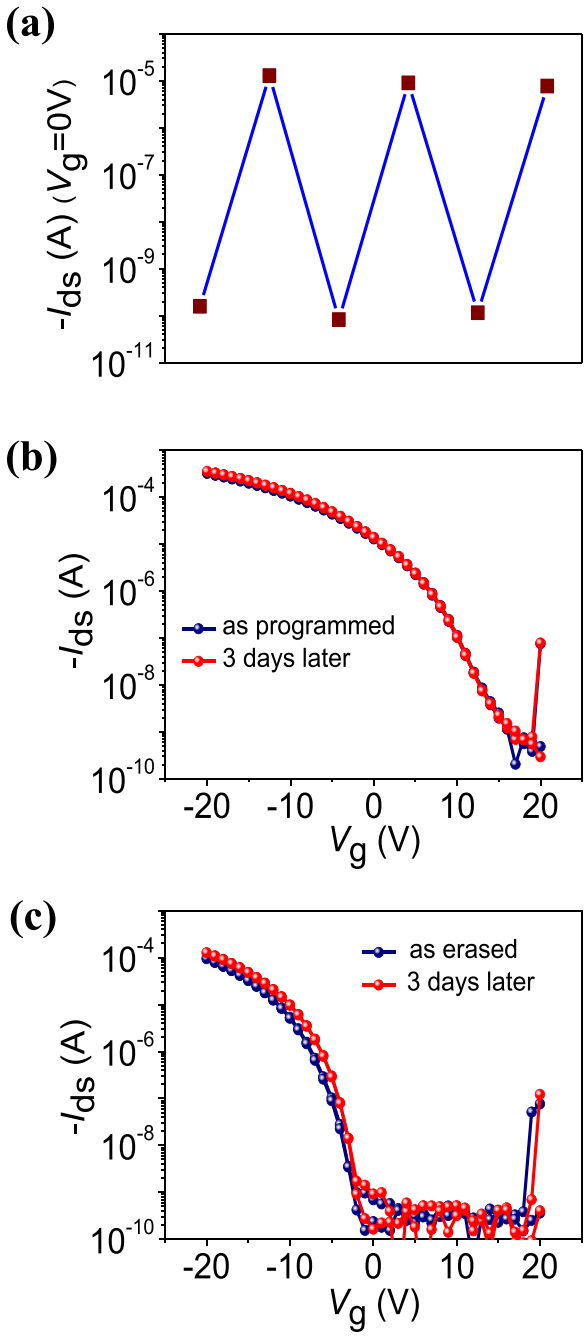

FIG. 3. Programming-erasing cycling and stability of P3HT/PS transistors. (a) I_{ds} at $V_g = 0$ for repeating programming-erasing cycling. (b) and (c) *In-situ* transfer characteristics for as-programmed (b), as-erased FET (c), and corresponding transfer characteristics after 3 days. All of the curved were measured at room temperature.

PS/SiO_2 interface so much that it matches that of P3HT, charge starts to accumulate at PS/SiO_2 interface. The critical V_g for charge accumulated within PS layer is

$$e|V_g| = \frac{|E_{P3HT} - E_{PS}|}{d_{PS}} \left(d_{SiO2} \frac{\varepsilon_{PS}}{\varepsilon_{SiO2}} + d_{PS} \right), \quad (3)$$

where e is element charge; E is the valence band; and ε is permittivity. From E_{P3HT}-$E_{PS} \approx 2.2$ eV, $d_{PS} = 20$ nm, $d_{SiO2} = 300$ nm, $\varepsilon_{PS} = 2.5$, and $\varepsilon_{SiO2} = 3.9$, we get a critical value for charge accumulation at the PS/SiO_2 interface, namely, $V_g = -23.4$ V, in agreement with the experimental results (Figure 2(e)). The chare injection from P3HT into PS is thermally activated.

The gate bias stress-induced change of V_t is reversible. As shown in Figure 2(f), the programming-erasing process yielded FETs with reliable transfer curves without hysteresis at room temperature, changing from accumulation to depletion mode and then backwards. The performance of programmed FETs is stable for all devices we studied, with retention time being longer than $>10^5$ s (Figure 3). This high stability is consistent with the fact that hysteresis-free performance dominates the transfer/output characteristics at room temperature, showing that the trapped charge is immobilized and not released during V_g/V_{ds} scanning. Longer retention time might be achieved using deeper traps in the insulator electrets, e.g., via chemically grafted polystyrene with side or end groups with high valence levels, or via blending the insulator polymer with small molecules or nanoparticles to form hybrid electrets.

As we discussed above, upon tuning the threshold voltage, the FET can be reversibly switched from enhancement to depletion mode operation. In Figure 4, we combined two P3HT/PS (5% P3HT) blend transistors, one programmed to work in the accumulation mode, and the other in the depletion mode to realize digital inverters. *In-situ* tuning threshold voltages of individual transistors shift output curves of the inverter along V_{in} direction.

In summary, we propose a method to *in-situ* tune the threshold voltage of P3HT/PS blend field-effect transistor, via applying a gate bias stress at elevated temperature. Charge injection from P3HT into PS matrix is thermally activated, and this charge is immobilized within the PS electret after cooling down to room temperature. The approach is applied to reversely tune the FET mode of operation from accumulation to depletion. Using FETs with different threshold voltages, we built digital converters with tunable performance.

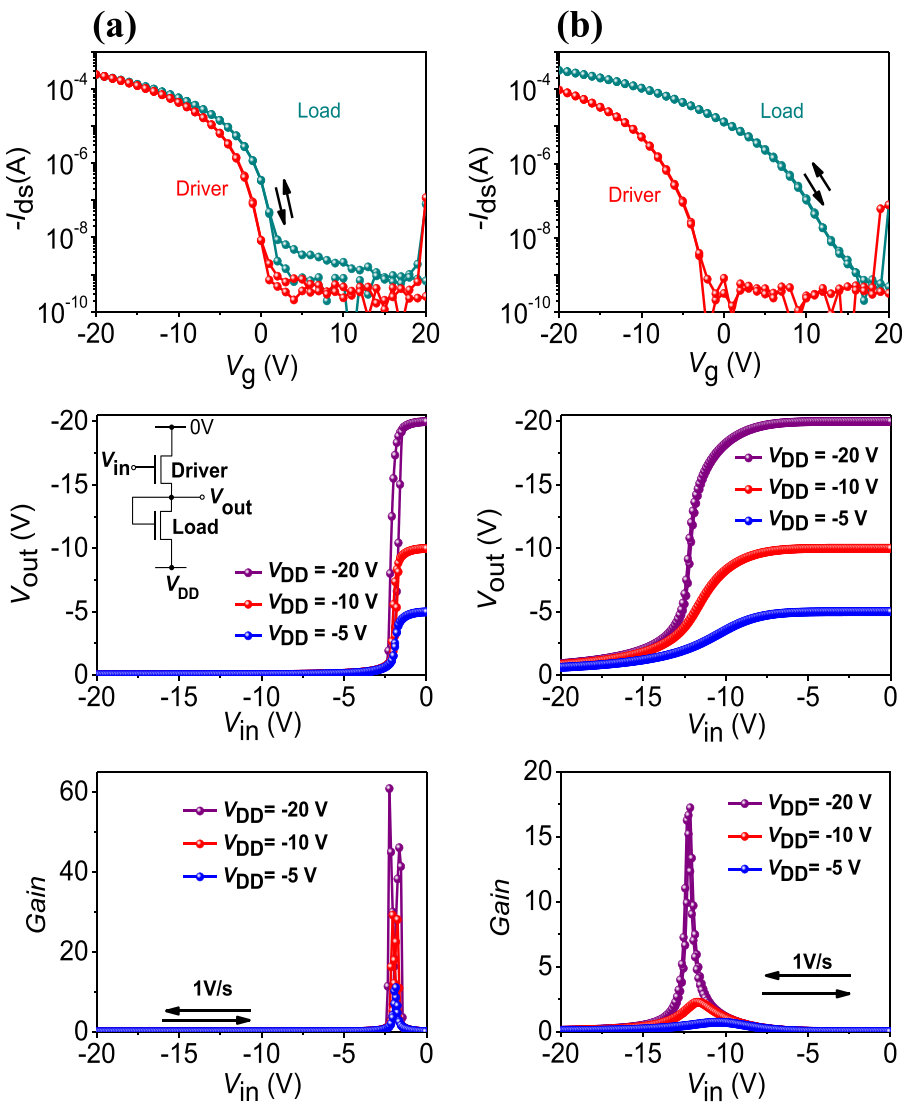

FIG. 4. *In-situ* tuning of V_t for circuit application. (a) Before programming; and (b) after programming. Top, transfer characteristics of driver and load FETs. Middle, the dependence of V_{out} on V_{in} of digital inverters. Bottom, corresponding gains of the inverters.

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