

Fraunhofer Challenges using FPGA Clusters HHI for Distributed CNN Training

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Abstract

easy-to-use An for attached FPGA clusters:

- **Training** of deep neural

Mapping a Network of Layers onto an FPGA Cluster



Problem

We need to find mappings of L layers to N FPGAs, represented as $d_{l,n,c} \in \{0,1\}$ with $0 \le l < L, 0 \le n < N, c \in C_l$, where $d_{l,n,c} = 1$ means layer l is placed on FPGA n with configuration c. C_l is the set of all possible configurations for layer l.

Each layer must be placed exactly once with one configuration.

$$\tilde{d}_{l,n} = \sum_{c \in C_l} d_{l,n,c}, \quad \sum_{n=0}^{N-1} \tilde{d}_{l,n} = 1 \quad \forall l < L, c \in C_l$$

These mappings need to respect the available resources $R_{n,t}^{dev} \in \mathbb{R}$ for each device n and resource type $t \in T$. For now, we consider the amount of **on-chip memory**, number of **DSP cores** and **DRAM bandwidth**. For each layer- and device type, we require estimates of the implementation's achievable throughput $S_{l,n}(c) \in \mathbb{R}$ and resource consumption $R_{l n t}^{\text{layer}}(c) \in \mathbb{R}$ depending on layer configuration С.

Strategy

(1)

Until now, we use binary search until the throughput is known to be within 5 % of the achievable throughput.

Simplified approach

- Select target throughput
- The optimization problem turns into a **Constraint Satisfaction Problem**
- Solvability check allows **binary search for max throughput**
- Pareto-optimal configurations considered for target throughput

Current further simplification

- Select one config per layer and device that meets target throughput
- Use achievable throughput as cost function

$$\sum_{l=0}^{L-1} \sum_{c \in C_l} d_{l,n,c} R_{l,n,t}^{\mathsf{layer}}(c) \le R_{n,t}^{\mathsf{dev}} \quad \forall n < N, t \in T$$
(2)

Additionally, we need to **consider the available network bandwidth** $C_n^{\text{dev}} \in \mathbb{R}$. The required bandwidth $C_{l,k}^{\text{layer}}(t)$ between layers l and k

can be calculated as $\hat{S}F_{l,k}$, where \hat{S} is the overall throughput and Fis the sum over all connections between l and k of the connection's feature map size.

$$\sum_{l=0}^{L-1} \sum_{k=0}^{L-1} \tilde{d}_{l,n} \left(1 - \tilde{d}_{k,n} \right) C_{l,k}^{\mathsf{layer}}(t) \le C_n^{\mathsf{dev}} \quad \forall n < N$$
(3)

Each network hop introduces some amount of latency, which can lead to stalls when two branches that have taken different paths across the cluster join. In order to avoid having to calculate and compensate for these delays, we require joining branches to have taken an equal **number of network hops** $H_l \in \mathbb{N}$ from the input.

$$H_{l} = H_{k} + \sum^{N-1} \tilde{d}_{l,n} \left(1 - \tilde{d}_{k,n} \right) \quad \forall l, k < L, F_{l,k} > 0 \quad (4)$$

- For convolutions, we use DSPs core usage
- For smaller clusters and models, solved using CP-SAT Solver (Google OR-Tools)
- Runtime issues with larger models and clusters
- Future considerations: Explore greedy, annealing, or deep learning methods

Model	Cluster	Plan F	Pinned	# Layers	FPS	Utilized DSPs
		L	ayers			
VGG mini	$2 \times 10AX115$	7 min	No	34	600	38.5%
Demo	$4 \times 10AX115$	3 min	No	127	558	72.2%
MobileNetV2	$4 \times AGFB014$	21 min	Yes	225	500	37.3%
		94 min	No	225	516	37.8%
	6 imes 10AX115	13 min	Yes	240	696	81.2%
		169 min	No	240	727	82.2%
ResNet18	All Devices	51 min	Yes	332	727	78.8%
		69 min	No	332	800	88.1%

A typical CNN Layer Combination for Training

n=0

Finally, we force input- and output layers onto FPGA 0.

 $\tilde{d}_{l.0} = 1 \quad \forall l \in P,$

where $P \subset \{0..L - 1\}$ is the set of input- and output layers. Given these constraints, we want to maximize the overall throughput S, which is equal to that of the slowest layer.

> maximize \hat{S} subject to Equations (1) to (5), $\hat{S} \le \sum \sum d_{l,n,c} S_{l,n}(c) \quad \forall l < L$ $n=0 \ c \in C_1$



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Forward

(5)

(6)